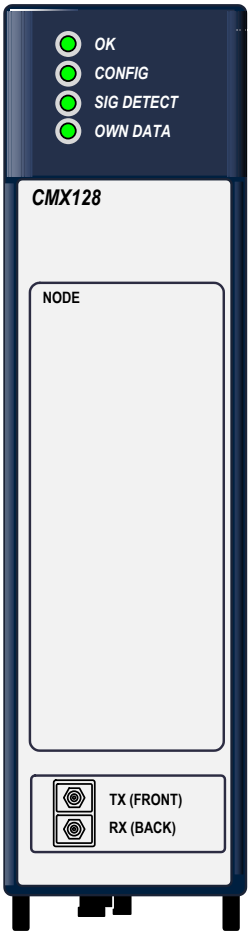
IMPORTANT PRODUCT INFORMATION

GFK-2506M

Sep 2019

PACSystems™ RX3i

CONTROL MEMORY XCHAGE MODULE (IC695CMX128)



EMERSON

Caution Notes as Used in this Publication

Caution

Caution notices are used where equipment might be damaged if care is not taken.

Notes: Notes merely call attention to information that is especially significant to understanding and operating the equipment.

These instructions do not purport to cover all details or variations in equipment, nor to provide for every possible contingency to be met during installation, operation, and maintenance. The information is supplied for informational purposes only, and Emerson makes no warranty as to the accuracy of the information included herein. Changes, modifications, and/or improvements to equipment and specifications are made periodically and these changes may or may not be reflected herein. It is understood that Emerson may make changes, modifications, or improvements to the equipment referenced herein or to the document itself at any time. This document is intended for trained personnel familiar with the Emerson products referenced herein.

Emerson may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not provide any license whatsoever to any of these patents.

Emerson provides the following document and the information included therein as-is and without warranty of any kind, expressed or implied, including but not limited to any implied statutory warranty of merchantability or fitness for particular purpose.

Introduction

The PACSystems Control Memory Xchange (CMX) module provides deterministic sharing of data among PLCs and other computing devices on a high-speed fiber optic network, using reflective memory technology. A reflective memory network can contain up to 256 nodes. Each node in the network can be any reflective memory device that is compatible with the 5565 family. When data is written to one node, all nodes on the network are automatically updated with the new data.

Each node in the reflective memory network is connected in a daisy-chained loop using fiber optic cables. The transmitter of the first node is tied to the receiver of the second. The transmitter of the second node is tied to the receiver of the third node, and so on, until the loop is completed back at the receiver of the first node. The figure on page 5 shows an example of a reflective memory network.

A PACSystems RX3i main rack supports a maximum of six CMX modules.

Features

- PACSystems RX3i single slot form factor.
- 128 Mbytes reflective memory with parity.
- Software configuration of all node parameters (no jumper or switch settings required).
- No RX3i CPU processing required to operate the network.
- Network-compatible with VMIC 5565 family of reflective memory devices, including the ACC-5595 reflective memory hub and the RX7i CMX module.
- Connection with multimode fiber up to 300m/984.25ft.
- Dynamic packet sizes of 4 to 68 bytes, controlled by the CMX module.
- Network transfer rate of 43 Mbyte/s (4 byte packets) to 174 Mbyte/s (64 byte packets)
- Network link speed of 2.1 Gigabits/sec.
- Programmable module interrupt output.
- Four general-purpose network interrupts with 32 bits of data each.
- Network error detection.
- Up to 256 nodes per network.
- Redundant transfer mode operation. This optional mode reduces the chance of a data packet being dropped from the network.
- Configurable network memory offset allows you to assign nodes on a network to groups according to the 16MB segment in the network address space that they use.

The CMX128 module must be located in an RX3i Universal Backplane. The module can be hot-inserted and removed following the instructions in the PACSystems RX3i System Manual (GFK-2314).

Specifications

Specification	Description
Packet size	Dynamic packet sizes of 4 to 68 bytes (firmware version 1.04 and later), automatically controlled by the CMX module
Transfer rate	Network link speed of 2.1 Gbits/sec
User memory	128MB SDRAM
Input power (from RX3i power supply)	660 mA @ +3.3 VDC 253 mA @ +5 VDC
Connectors	▪ Fiber optic LC type, conforms to IEC 61754-20 ▪ Zirconium ceramic ferrule ▪ Insertion loss: 0.35 dB (maximum)

Specification	Description
	▪ Return loss: -30dB

Refer to the PACSystems RX3i System Manual (GFK-2314) for product standards and general specifications.

Related Publications

Available at https://www.emerson.com/Industrial-Automation-Controls/support.

PACSystems Memory Xchange Modules User's Manual (GFK-2300)
PACSystems RX3i System Manual (GFK-2314)

PACSystems Installation and Maintenance Requirements (GFK-2975) or later
PACSystems CPU Reference Manual (GFK-2222)
PAC Machine Edition Logic Developer-PLC Getting Started (GFK-1918)

Ordering Information

Description	Catalog Number
Control Memory Xchange Module for RX3i	IC695CMX128
Fiber-optic Cables	VMICBL-000-F5-0xx, where 0xx distinguishes different lengths
Reflective Memory Hub	VMIACC-5595

Installation and Maintenance

Refer to PACSystems Installation and Maintenance Requirements (GFK-2975) to ensure safe use guidelines are followed for each installation environment.

Quick Guide to CMX Operation

The CMX module initially powers up in an unconfigured state with its optical transmitter and receiver disabled. The module cannot operate on a network until the RX3i CPU has delivered a hardware configuration to the module.

Basic operating functions are configured using Machine Edition – Logic Developer PLC. You can configure the following parameters in the hardware configuration: Node ID, Redundant Transfer Mode, Rogue Master, Network Memory Offset, and Interrupt enable.

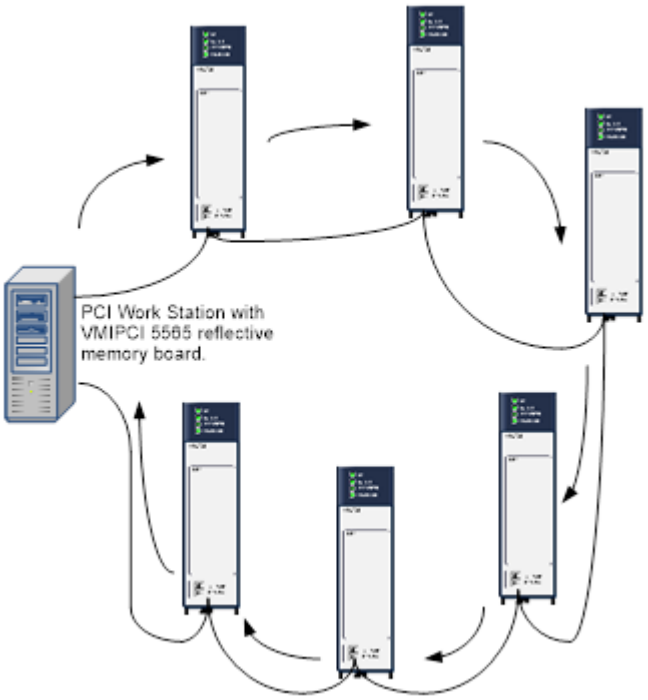
Additional functions beyond the basic read and write operations, including enabling interrupts, reading interrupt status, enabling parity, and reading parity errors, can be performed by user logic. For details on accessing these advanced functions, refer to the PACSystems Memory Xchange Modules User's Manual, GFK-2300.

Once the CMX has been configured, a transfer of data over the network can be initiated by writing to the reflective memory region through the backplane. The CMX forms the data into variable length packets sized from 4 to 68 bytes, which it transmits over the fiber-optic network to the receiver of the next node. Whenever a packet is received, the CMX evaluates the packet. If the packet is valid and did not originate on this node, it is accepted. If, however, the data packet is invalid or if it originated at this node, it is discarded. The receiving node writes the data into the local reflective memory and simultaneously transmits the data to the next node on the network. The process is repeated until the data returns to the originating node, where it is removed from the network.

Sample Reflective Memory Network

The seven-node network in the following illustration consists of six RX3i CMX modules and a PCI WorkStation with a VMIPCI 5565 reflective memory board.

Figure 1: Reflective Memory Network

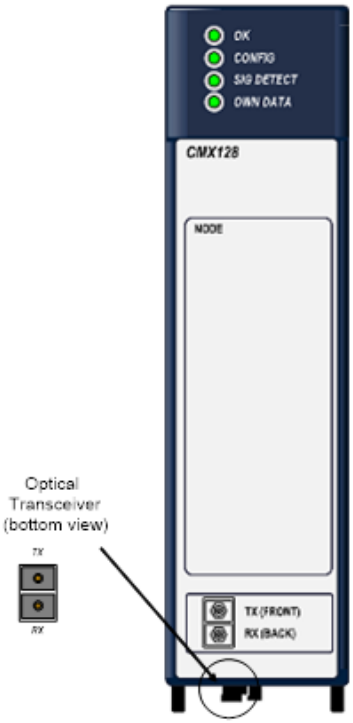


Optical Transceiver

The optical transceiver, which is located on the bottom of the module, has two "LC" type fiber optic ports. The port labeled "TX" is the transmitter and the port labeled "RX" is the receiver.

CMX modules are networked together using either simplex (single fiber) or duplex (dual fiber) multimode fiber optic cables. The specific cable construction depends on your operating environment. For details on cables, refer to the *PACSystems Memory Xchange Modules User's Manual,* GFK-2300.

Figure 2: Optical Transceiver



LEDs

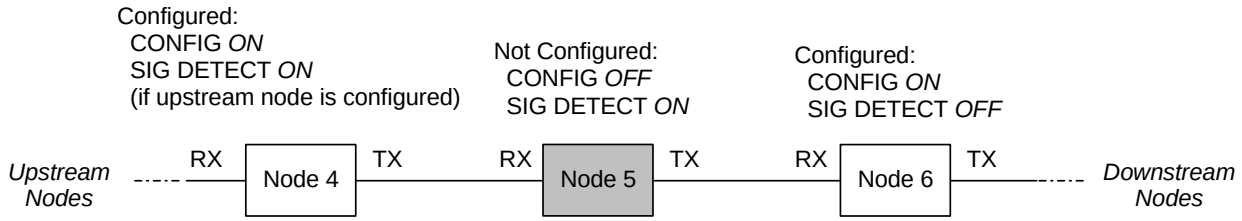
All front panel LED indicators are green.

LED Label	Description
OK	ON indicates the CMX module and the CPU are functioning properly.
CONFIG†	ON indicates the module is configured.
SIG DETECT	ON indicates the receiver is detecting a fiber optic signal.
OWN DATA	ON indicates the module has received its own data packet from the network at least once.

Note: A reflective memory hub can be used to bypass a node that is not configured.

Example of SIG DETECT Operation -- Node 5 Not Configured

Figure 3: SIG Detect Operation



Release History

Module Version	Firmware Version	Date	Comments
IC695CMX128-GH	2.01	Sep 2019	Following Emerson's acquisition of this product, changes have been made to apply appropriate branding and registration of the product with required certification agencies. No changes to material, process, form, fit or functionality.
IC695CMX128-FH	2.01	Mar 2016	**Hardware change:** Power Cycle issue that in rare cases after cycling power on the module could result in "loss of module" during power up. A subsequent power cycle will clear this condition. Refer to the section Problems Resolved by Hardware version -Fx for additional information. **Firmware version 2.01:** In rare cases a timing issue occurs after a power cycle resulting in a "loss of module" during power up. A subsequent power cycle will clear this condition. Refer to the section *Problems Resolved* for additional information.
IC695CMX128-EG	2.00	Jul 2015	This change just further enhances the designs' resistance to the rare condition of corruption during a memory read from occurring.
IC695CMX128-DG	2.00	Sep 2013	Hardware update to resolve a component obsolescence issue. No changes to features, functions or compatibility.
IC695CMX128-CG	2.00	Jul 2013	This update prevents a rare memory read data corruption issue from occurring.
IC695CMX128-BF	1.07	Feb 2013	This firmware update enhances the data corruption self-correcting mechanism to provide additional detection and correction capability for memory reads.
IC695CMX128-BE	1.06	Dec 2012	This hardware update addresses a rare condition in which some units may exhibit an impedance between system 0V and earth ground that is lower than the designed value.
IC695CMX128-AE	1.06	Oct 2012	The mechanism used to report the memory read data corruption via the parity error LISR bit and interrupt has been removed in version 1.06 in favor of a new self-correcting mechanism that is transparent to the user application and handled internally by the CPU (beginning with CPUv7.17).
IC695CMX128-AC	1.04	Aug 2011	Increases the maximum packet size that can be accepted and processed to 68 bytes.

Module Version	Firmware Version	Date	Comments
			Adds the ability to detect and correct a rarely occurring condition of corruption in data read operations.
IC695CMX128-AB	1.02	Oct 2009	See GFK-2506B for problems resolved.
IC695CMX128-AA	1.00	Sep 2008	Initial release.

Important information for this release

Upgrades

⚠ Caution

- Do not install firmware version 2.00 or later on hardware versions –Ax or –Bx. This will render the unit inoperable and will require the unit be returned to the factory.

Functional Compatibility

The CMX128 requires the following versions for configuration and operation.

Subject	Description
Programmer Version Requirements	PAC Machine Edition Logic Developer 5.80 (released build 4541) or later is required to use the RX3i IC695CMX128 modules.
RX3i CPU	RX3i CPU firmware version 7.75 (or later) is required to be used with CMX128 hardware version 2.00 or later (–Cx and later) and firmware version 2.00 or later.
CMX128 Versions	Firmware version 2.00 is not compatible with earlier hardware versions. Firmware versions earlier than 2.00 are not compatible with 2.00 and later (-Cx and later) hardware versions.
Rack Location	The CMX128 must be located in the main RX3i rack. IC695CMX128 modules require a PCI backplane, which is not available on IC694CHSxxx expansion bases.

Problems Resolved with this Release

None

Restrictions and Open Issues in this Release

Subject	Description
RX3i RMX/CMX modules require grounded ESD strap for EMC Installation	When installing, operating, or maintaining the IC695CMX128, personnel must insure any electrostatic charge is discharged through the use of a grounded ESD strap or other means to meet IEC-61000-4-2 (ESD) requirements. A direct electrostatic discharge event of 4kV or higher applied to the metal optical transceiver housing may result in a lights out module requiring a power cycle to recover.
RX3i RMX and CMX modules require a metal enclosure to meet radiated emissions requirements.	For installation requirements, see “Government Regulations”

Subject	Description
RX3i CMX/RMX does not disable transmitter when the CPU goes to Stop/Halt mode.	For CMX128 modules and RMX128 modules not used as redundancy links, the automatic transmitter disable feature currently does not work correctly when a controller goes to Stop/Halt mode. When the CPU goes to Stop/Halt mode or fails and the automatic transmitter disable feature is enabled, the fiber optic transmitter should be turned off, breaking the reflective memory link. When the feature is disabled the transmitter remains ON and the reflective memory link will not be broken. When enabled, the automatic transmitter disable feature does not work when the CPU goes into Stop/Halt mode (such as after a software watchdog trip or multi-bit ECC error detection), leaving the fiber optic transmitter ON. The fiber optic transmitter is properly disabled if the CPU fails or is lost (for instance the CPU hardware is removed, the CPU experiences a hardware watchdog event, or displays a blink code such as a page fault). This user-configurable feature is enabled by default. It may be disabled by clearing bit 12 with a BUS_WRITE to region 3, offset 0x440.
The LCSR status bit is not turning ON after LISR turns ON when Interrupt (Sync Loss) is generated	The LCSR bit is not latched to the ON state (indicating sync loss) and should not be used for sync loss detection. The LISR bit should be used for detecting sync loss.
SVC_REQ 17 is not supported	SVC_REQ 17 is not supported to mask or unmask module interrupts on RX3i CPUs. There is currently no way to identify which module interrupt should be masked on RX3i. To turn off interrupts, use the normal interrupt disabling mechanism described in the IC695CMX128 user's manual. For details, see “Dynamic Masking of Interrupts” in the PACSystems Memory Xchange Modules User’s Manual, GFK-2300.

Operational Notes

Subject	Description
Bad Data Interrupt	To prevent continuous interrupts when the Bad Data Interrupt is enabled, you may want to temporarily set bit 8 in the LIER to 0 when a sync loss condition is detected. If your application is also using the Sync Loss Interrupt, you may also want to temporarily set bit 11 in the LIER to zero when the sync loss condition is detected. You can then re-enable the Bad Data Interrupt (and Sync Loss Interrupt if it was also disabled) when the sync loss condition has been corrected.

Technical Support & Contact Information

Home link: http://www.Emerson.com/Industrial-Automation-Controls

Knowledge Base: https://www.emerson.com/Industrial-Automation-Controls/support

Note: If the product is purchased through an Authorized Channel Partner, please contact the seller directly for any support.

Emerson reserves the right to modify or improve the designs or specifications of the products mentioned in this manual at any time without notice. Emerson does not assume responsibility for the selection, use or maintenance of any product. Responsibility for proper selection, use and maintenance of any Emerson product remains solely with the purchaser.

EMERSON