January 2010
GFK-0702AC

IMPORTANT PRODUCT INFORMATION

READ THIS INFORMATION FIRST

Product: IC693 CPU Firmware Release 8.40
IC693CPU311-AD, AE
IC693CPU313-U, V
IC693CPU323-U, V
IC693CPU331-CE
IC693CPU341-W

Introduction

This document contains information that is not available in any other publication; therefore, we recommend you save it for future reference.

This document discusses a new feature released in firmware version 8.40 for the five CPU modules listed above, and also contains information on previous release 8.21.

This document is revised to correct an error in the previous version (AB), which stated that firmware version 8.21 supports the DSM314 motion module. IC693 CPUs with firmware version earlier than 10.0 ***do not*** support DSM314.

New Features and Functionality of Firmware Release 8.40

Firmware release 8.40 adds the Ignore Fatal Fault feature to the five CPUs listed above. This feature is enabled/disabled with a new configuration parameter. When set to Enabled, the CPU will ignore, during power-up, any active PLC error mode condition. If enabled, this feature also requires the Power-up Mode parameter be set to Run or Last. If this feature is enabled, and a running CPU goes into Stop/Fault mode, the CPU can be started back up in Run mode by power-cycling the PLC. (Previously, it was necessary to use programming software or a Hand-Held Programmer to restart a CPU that had gone into Stop/Fault mode.) When it powers back up, the CPU will ignore the current error mode condition and proceed to the previous operating mode (Run/Stop). This parameter has no effect on the detection and logging of faults. The default setting for this parameter is Disabled. This feature is useful in applications where the PLC experiences a nuisance fault, such as due to noise from a nearby electrical storm, and no support person is on-site to restart it; however, there may be applications where it is not safe to use this feature, so read the warning below.

To configure this feature, you must use CIMPLICITY Machine Edition software, VersaPro 1.1 or later, or the MS DOS®-based programming software, version 9.03 or later. This feature is not supported in the Hand-Held Programmer.

Users with earlier versions of these CPUs who would like to use this new feature may upgrade these earlier CPUs to firmware release 8.40 (see the heading “Firmware Upgrade Kits”).

Warning

The Ignore Fatal Fault feature should not be used (should be set to *Disabled*) in applications where a restart under fault conditions could produce an unsafe condition in the controlled equipment. It is the responsibility of the system designers to determine whether this feature can be used safely with their equipment. Failure to follow this warning could result in injury or death to personnel and/or damage to equipment.

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Hardware Identification

PLC Model	*Board ID*	*Board Revision*
IC693CPU311	BC3C2	44A731725-G01R02 or later
IC693CPU313	BC3C2	44A731725-G01R02 or later
IC693CPU323	BC3D2	44A731730-G01R04 or later
IC693CPU331	CP3A3	44A737299-G01R03 or later
IC693CPU341	CH3A2	44A735369-G01R03 or later

Note: The newer suffixes (AE, V, and V) shown in the product list at the top of page 1 indicate a change in the way the memory backup battery is shipped and does not affect the products' features and functionality. For additional details on the memory backup battery, please see GFK-1948B or later.

Firmware Identification

Firmware for these CPUs is stored in a replaceable EPROM. The following table provides identification information for this EPROM.

Current CPU Catalog Number	*Previous Catalog Numbers Replaced by this Release*	*EPROM Location*	*EPROM Label*	*Checksum*
IC693CPU311AD, AE	IC693CPU311AC and earlier	U8	395-027M 8.40	01CBE1A8
IC693CPU313U, V	IC693CPU313T and earlier	U8	395-018M8.40	01CD6761
IC693CPU323U, V	IC693CPU323T and earlier	U8	395-019M 8.40	01CD6761
IC693CPU331-CE	IC693CPU331-CD and earlier	U35	395-045D 8.40	01BBA5B0
IC693CPU341W	IC693CPU341V and earlier	U35	528-001P 8.40	01AFA77C

Firmware Upgrade Kits

Those wishing to upgrade earlier versions of these CPU modules to version 8.40 may purchase the appropriate upgrade kit. Select the upgrade kit catalog number that corresponds to your CPU from the following table. Before upgrading firmware, read the "If Upgrading Firmware" note in the "Operational Notes" section of this document.

CPU Model	*Upgrade Kit Catalog Number*
IC693CPU311	44A731233-G16
IC693CPU313	44A731249-G12
IC693CPU323	44A735538-G12
IC693CPU331	44A731232-G16
IC693CPU341	44A731240-G13

Operational Notes

If Upgrading Firmware

The user program, configuration, CPU ID (used for SNP communication), and status tables will automatically be cleared when the CPU firmware EPROM is changed. So you will need to restore these after performing a firmware upgrade. The user program, configuration, and status tables can be restored from a program folder, from memory card, or EEPROM. The SNP ID must be set separately using the MS-DOS PLC programming software, VersaPro software, or the Hand-Held Programmer.

EM3 Compatibility

All IC693 Ethernet Interface (IC693CMM321) modules used with release 6.50 or later of the IC693 PLC should be updated to release 1.10 or later of the IC693CMM321. The MS-DOS PLC programming software (IC693 TCP/IP/Ethernet) requires both CPU release 6.50 or later and IC693CMM321 release 1.10 or later.

During a Run Mode (alt-s) Program Store of a large program block (greater than 14 kilobytes), the EM3 may time-out, causing communications to fail. Changing the Communication Window to Run-to-Completion mode, or storing the program in stop mode, will allow the store to take place successfully.

FBC Compatibility

The FBC version 3 or later is required for release 8.00 or later of the IC693 PLC CPU firmware.

Problems Resolved by This Firmware Release (8.40)

Time-of Day (TOD) Clock Start-up Problem on CPU331 and CPU341

In some cases, if the backup battery was disconnected after the CPU was powered down, the TOD clock would not restart when the PLC was powered back up. This would result in a fatal fault being logged that identified the failure of the TOD clock. Subsequent cycling of power would not cause the clock to restart. It could be restarted, however, by removing the CPU and shorting the “super capacitor” memory backup capacitor. This problem has been corrected in firmware release 8.40. (Note that CPUs 311, 313, and 323 do not have a TOD clock.) Users with earlier versions of CPU331 or CPU341 who experience this problem are advised to upgrade these CPUs to firmware release 8.40 (see the heading “Firmware Upgrade Kits”).

Problems Resolved by Prior Firmware Release 8.21

FBC Editing with Hand Held Programmer (HHP)

A soft alarm fault could occur in release 8.20 when editing an FBC configuration with a hand held programmer. This problem has been corrected in release 8.21.

Storing Foreign Module Configuration to Slot 1

Storing a configuration with a foreign module in slot 1 (possible only on 311, 313, or 323) would result in a fatal fault in release 8.20. This has been corrected in release 8.21.

End Function Block

The End Function Block no longer terminates a sweep if it is in a subroutine. It merely exits the subroutine. This restores the functionality as it was prior to release 8.

SVC REQ7

SVC REQ 7 previously would allow an invalid date, such as 2/29/01 to be entered. Dates with a day number greater than is legal for the specified month is no longer allowed as input to SVC REQ 7.

Additions to User Manual

The following will be added to the *IC69* PLC Serial Communications User's Manual* at its next revision (version E):

Disable Break-Free SNP Slave Operation COMMREQ: 7004

Available Modes: Slave
Description:

Local command. This command disables the break-free SNP feature in IC693 CPU firmware version 8.20 and later versions. Break-free SNP simplifies MODEM communication with IC693 PLCs by eliminating the requirement for a serial break at the start of each SNP and SNP-X session.

Break-free SNP on built-in slave ports in PLC CPUs uses a small fraction of the CPU processing bandwidth. For most applications the impact on CPU performance is negligible. However, applications that use multi-drop SNP or SNP-X communication can incur noticeable increases in PLC sweep times because all slave units must examine every received message.

This command disables break-free operation and eliminates its impact on PLC sweep time. Break-free operation remains disabled until the next time the PLC is powered on or command 7005 is executed. If a communication session is in progress when the command is executed, communication will continue, but detection of no-break Attach/X-Attach messages will stop immediately.

The COMMREQ that sends this command may be executed on the first PLC sweep.

If the COMM_REQ status word location specified in words 3 and 4 of the command block is not a valid %R, %AI or %AQ reference, power flow into the COMM_REQ function block will cause power flow to its fault (FT) output. Otherwise, the value one (1) is written to the status word when the command succeeds. When unsuccessful, one of these values is returned:

010Ch	WAIT-mode COMREQ is not permitted; must use NOWAIT.
020Ch	Command not supported; the port is either not configured as an SNP slave or does not support break-free operation.

Sending this command when break-free SNP is already disabled has no effect; however, the COMMREQ status location will be set to 1, indicating success. Sending this command to a PLC CPU built-in serial port that does not support break-free SNP will set the fault output of the COMMREQ.

COMMREQ Parameters:

SYSID:	**IC693CPU311, IC693CPU313, IC693CPU323:**	0	(0000)
	IC693CPU331, IC693CPU341:	1	(0001)
Task:		00031	(001F)

Example Command Block:

Word 1:	00001 (0001)	SNP Data Block Length
Word 2:	00000 (0000)	NOWAIT Mode
Word 3:	00008 (0008)	Status Word Memory Type (%R)
Word 4:	00000 (0000)	Status Word Address minus 1 (Register 1)
Word 5:	00000 (0000)	Not Used
Word 6:	00000 (0000)	Not Used
Word 7:	07004 (1B5C)	SNP Command Number: Disable break-free SNP

Enable Break-Free SNP Slave Operation COMMREQ: 7005

Available Modes: Slave
Description:

Local command. This command enables the break-free SNP feature in IC693-30 CPU firmware version 8.20 and later. See command 7004 for a discussion of break-free SNP.

Because break-free operation is enabled when the PLC is powered on, this command has no effect unless command 7004 was previously executed. If a communication session is in progress when this command is executed, communication will continue, and detection of no-break Attach/X-Attach messages will begin when the current session is ended by a link-idle time-out.

The COMMREQ that sends this command may be executed on the first PLC sweep.

If the COMM_REQ status word location specified in words 3 and 4 of the command block is not a valid %R, %AI or %AQ reference, power flow into the COMM_REQ function block will cause power flow to its fault (FT) output. Otherwise, the value one (1) is written to the status word when the command succeeds. When unsuccessful, one of these values is returned:

010Ch	WAIT-mode COMREQ is not permitted; must use NOWAIT.
020Ch	Command not supported; the port is either not configured as an SNP slave or does not support break-free operation.

Sending this command when break-free SNP is already enabled has no effect; however, the COMMREQ status location will be set to 1, indicating success. Sending this command to a PLC CPU built-in serial port that does not support break-free SNP will set the fault output of the COMMREQ.

COMMREQ Parameters:

SYSID:	**IC693CPU311, IC693CPU313, IC693CPU323:**	0	(0000)
	IC693CPU331, IC693CPU341:	1	(0001)
Task:		00031	(001F)

Example Command Block:

Word 1:	00001 (0001)	SNP Data Block Length
Word 2:	00000 (0000)	NOWAIT Mode
Word 3:	00008 (0008)	Status Word Memory Type (%R)
Word 4:	00000 (0000)	Status Word Address minus 1 (Register 1)
Word 5:	00000 (0000)	Not Used
Word 6:	00000 (0000)	Not Used
Word 7:	07005 (1B5D)	SNP Command Number: Enable break-free SNP